Remarks

In response to section 1, "Claim Objections", of the office action, the Examiner is asked to note that claim 4 has been amended to include a period at the end.

In light of the Examiner's observations contained in section 1, "Specification", of the office action, the Examiner is referred to the above mentioned amendments of the specification in which he will note that the Applicant has made a number of changes to the numerals referred to in page 7 of the description as originally filed, which will render the description in conformity with Figure 2 of the drawings. Two further corrections to the descriptions at page 6, line 18 and page 7, line 9 are requested which correct errors which, it is respectfully submitted, are apparent and which have no substantive effect on the content of the description.

Referring now to sections 2-5, "Claim rejections" of the office action, it is noted that the Examiner has rejected independent claims 1, 9 and 17 under 35 U.S.C. §102 as being anticipated by Quay (US 6,115,360) and further rejected claims 2, 3, 10 and 11 under 35 U.S.C. §103 as being unpatentable over Quay. While these two sets of claims (1, 9 and 17 on the one hand and 2, 3, 10 and 11 on the other hand) have been rejected on different grounds, the Applicants will deal with the rejection of these sets of claims at the same time.

The Examiner is asked to note at this stage that all of the independent claims (1, 2, 9, 10 and 17) have each been amended to clarify that the present invention relates to methods and interface arrangements for interfacing frame based **TDM** telecommunications traffic from a framed based **TDM** network to an asynchronous network.

The Examiner has contended that Quay teaches a method and apparatus for interfacing frame-based telecommunications from a frame-based network (SONET, Figure 2 box 20) to an asynchronous network (Figure 1, boxes 5, 8). The Examiner then goes on to indicate that the method taught by Quay further comprises mapping

the frame based traffic into cells or packets and scheduling the despatch of the cells into the asynchronous network at a substantially constant rate.

There is a contradiction at the heart of the Examiner's contention. Quay relates to a network hub and asynchronous transfer node (ATM) translator system (5) for use in a local area network (LAN)–based communication system. As such, the system comprises a host controller 10 acting as the LAN network hub and an ATM translator 5, including a translator card 15, which interfaces with a local bus (PCIBUS) and which includes circuitry for performing LAN to ATM translation and for interfacing to a fiber optic facility (FO). The translator card 15 includes a segmentation and reassembly (SAR) device 12 which is connected via a local bus (LBUS) to SONET receive/transmit circuitry 20 which encodes and decodes the communications according to the well-known SONET standard. SONET receive/transmit circuitry 20 is in turn connected to transceiver 22, which drives signals onto the fiber optic facility (FO) and receives signals therefrom, in the conventional manner (column 5, lines 9-46). It is abundantly clear from this part of the disclosure of Quay, and indeed from the whole of the disclosure of this prior art reference, that Quay is directed to a system which translates LAN Ethernet frames to ATM cells, said frames being translated into ATM cells which are, subject to a scheduling process, transmitted on the ATM part of the system. The ATM cells are then communicated in a conventional manner over a standard SONET fiber optic network. This then is the contradiction in the Examiner's contention as to the teaching of Quay. Quay does not suggest translating SONET frames into an ATM format for scheduling and transmission. It is accepted by the Applicant that the SONET receive/transmit circuitry 20 of Quay is capable of receiving, on its receive function, SONET type traffic which it converts to ATM packets for communication to the computer devices of the LAN network. However, there is no suggestion whatsoever that the scheduling process taught in Quay is applied when the SONET traffic is converted to ATM packets in the receive direction. It is therefore not possible for the Examiner to sustain his contention that Quay teaches a method and apparatus for interfacing frame based telecommunications from a frame based SONET type network to an asynchronous network including a scheduling process. Thus, one distinction of the

present invention as defined by the amended independent claims is that the present invention relates to a method of interfacing TDM (SDH, SONET or PDH, for example) telecommunications traffic over an asynchronous (ATM, for example) network. Contrast this to that taught in Quay which teaches translation of Ethernet LAN frames to ATM cells and for the ATM cells to be converted to SONET in a conventional manner for onward transmission.

A further important difference between the present invention as defined by the newly amended independent claims over that of Quay and already touched upon above is that the present invention is directed to processing TDM telecommunications traffic rather than Ethernet LAN traffic. In an Ethernet LAN, all stations (computers (2) in Quay) are attached to the Ethernet and are connected to a shared signalling system. Ethernet signals are transmitted serially, one bit at a time, over the shared signal channel to every attached station. To send data, a station first listens to the channel, and when the channel is idle the station transmits data in the form of an Ethernet frame, or packet. After each frame transmission, all stations on the network must contend equally for the next frame transmission opportunity. This ensures that access to the network channel is fair, and that no single station can lock out the other stations. Access to the share channel is determined by medium access control (MAC) mechanism embedded in the Ethernet interface located in each station. This contrasts with a TDM system in which frames are multiplexed on a time basis rather than on a contention basis. This is an important difference between the present invention and the disclosure of Quay since it relates to the ability of the present invention to map the frame based TDM traffic into cells or packets and to schedule the despatch of these cells or packets into the asynchronous network at a substantially constant rate using what is in effect a fairly simple credit mechanism based on a simple clock system linked to the TDM frame rate. Reference is made to page 6, lines 17-30 of the specification of the present invention in which is described the simple frame clock 51 used to provide the synchronous timing mechanism required to control the scheduler process of the present invention. The following description at page 6, line 32 onwards explains how credits are issued to data structures in proportion to the data structures rate of data generation which is the

means by which data structures assembled into cells or packets are despatched into the asynchronous network. Compare this to the system disclosed in Quay which describes a fair scheduling scheme for available bit rate (ABR) asynchronous transfer mode transmissions (column 3, lines 19 and 20) where ABR is described as comprising explicit flow control indications in data cells used by the source network node to dynamically control its transmission rate in response to current network conditions where such control is affected within certain transmission parameters. Typically, source and destination nodes agree upon peak and minimum cell rate transmission conditions (column 2, lines 27-37 of Quay). By its very nature, Quay is not a system which is seeking to despatch cells or packets at a substantially constant rate and it can be understood from the scheduling mechanism discussed in Quay that the function of the scheduler is to provide a fair scheduling scheme rather than a substantially constant rate scheme, refer to Quay column 3, lines 40-48 and column 8, line 26 to column 9, line 17. It is clear from this part of Quay that the scheduling function uses a complicated addition and sort ahead process to determine when in the future to schedule the despatch of a cell in contrast with the simple clock tick system of the present invention which results in the ability of the present invention to despatch cells or packets into the asynchronous network at a substantially constant rate.

In view of the above, it is respectfully submitted that the present invention as defined by amended independent claims 1, 4, 9, 10 and 17 is patentably distinct from that disclosed in Quay and that consequently the claims of this application are in order for allowance.

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Respectfully submitted,

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Version With Markings Showing Amendments Made

Specification

Page 6, lines 17 – 30:

A Frame Clock 51 is used to provide the synchronous timing mechanism required to control the scheduler process. Typically the clock is [be] used to provide two levels of timing control, the frame signal and the intra-frame timing signal, here referred to as a tick. The frame signal as its name implies is used to provide a periodic framing signal. For example, in the case of PCM voice this framing signal would be generated once every 125 μs corresponding to the frame rate. The intra-frame timing signal or tick is used to provide timing within the frame, the resolution of the tick being at least equal to the number of synchronous data channels supported by the device. For example a scheduler designed to schedule the assembly of 8000 synchronous data channels into a number of data packet structures would require at least 8000 ticks per frame. In reality the number of ticks may be set to slightly larger than the number of synchronous data channels, the additional 'ticks' providing tolerance or slack within the basic scheduling algorithm to enable housekeeping and other control tasks to be interleaved within the basic scheduling algorithm.

Page 7, lines 5 – 33:

The rate of generation of credits and the intervals within the frame period at which each credit is issued is determined by a reverse channel map [53] 23. The reverse channel map contains one location of memory per synchronous data channel supported by the scheduler device. Thus in the 8000 channel example the table would contain 8000 [channels] locations. Each location of the map contains the identity of the data structure to be credited. The scheduler creditor process 52 reads the map in a cyclic manner driven by the frame clock ticks so that each location of the map is read exactly once per frame.

A connection control process [55] 2 is used to configure and control the reverse channel map [53] 23. At scheduler initialization, all locations within the map [53] 23

are set to null to indicate that there is nothing at present to schedule. To begin scheduling the assembly of a data structure the connection control process [55] 2 assigns credits to that data structure by writing its identity into free locations in the map [53] 23. The number of locations, i.e. credits, assigned to the data structure is directly proportional to its data rate. The locations that are assigned to the data structure dictate, within the frame interval the timing distribution for the assembly of its credits. Therefore the algorithm that the connection control process uses to assign free locations to a data structure will dictate the scheduling distribution for that structure. The scheduler process described will support any chosen algorithm for this process. The appropriate algorithm may thus be selected to suit the desired timing solutions for a particular application. Potential options for the allocation of free slots include but are not limited to the following.

The connection control process [55] 2 uses a substantially random process to allocate free slots to the data structures. Particularly for large data structures where the number of data channels is greater than the nominal packet size, this will tend to ensure overall a random scheduling of packets within the frame interval and thus provides an effective mechanism to limit jitter.

Claims

1. (Once amended) A method of interfacing frame based time division multiplex (TDM) telecommunications traffic from a frame-based TDM network to an asynchronous network, the method comprising mapping the frame-based TDM traffic into cells or packets, and scheduling the despatch of said cells or packets into the asynchronous network at a substantially constant rate.

2. (Once amended) A method of interfacing frame based TDM telecommunications traffic in which each TDM frame supports a plurality of data structures each comprising one or more channels from a frame-based TDM network

to an asynchronous network in which traffic is transported in cells or packets, the method comprising;

issuing credits at a substantially constant rate;

assigning the credits to each said data structures according to the size of that data structure;

determining for each said data structure a threshold number of assigned credits; and,

when said threshold value is reached, assembling that data structure into cells or packets for despatch into the asynchronous network.

4. (Once amended) A method as claimed in claim 3, wherein said connection control assigns credits to a data structure by writing the identity of that data structure into free locations in a reverse channel map.

9. (Once amended) An interface arrangement for interfacing frame based TDM telecommunications traffic from a frame-based TDM network to an asynchronous network, the arrangement being arranged to map the frame-based TDM traffic into cells, and incorporating a scheduler for scheduling the despatch of said cells into the asynchronous network at a substantially constant rate.

10. (Once amended) An interface arrangement for interfacing frame based TDM telecommunications traffic in which each TDM frame supports a plurality of data structures each comprising one or more channels from a frame-based TDM network to an asynchronous network in which traffic is transported in cells or packets, the method comprising;

means for issuing credits at a substantially constant rate;

means for assigning the credits to each said data structures according to the size of that data structure; and

means for determining for each said data structure a threshold number of assigned credits whereby, when said threshold value is reached, the data structure is assembled into cells or packets for despatch into the asynchronous network.

17. (Once amended) A method of scheduling despatch of a TDM data structure packetized into cells or packets for despatch into an asynchronous network, the method comprising allocating credits to the data structure at a predetermined rate, comparing the accumulated total of credits for said data structure, and, when said total reaches a predetermined threshold, despatching said cells into the asynchronous network at a substantially constant rate.